REMARKS

Applicant hereby adds new claims 61-80 and cancels claims 51-60. Accordingly, claims 21-30 and 61-80 are pending in the present application.

Claims 21-30 stand rejected under 35 USC 102 for anticipation by U.S. Patent No 5,821,591 to Krautschneider et al. (the '591 reference).

Applicant respectfully traverses the rejection and urges allowance of the present application.

Referring to the continued rejection of claim 1 over the '591 reference, Applicant respectfully requests clarification of the '591 teachings relied upon in support of the rejection if claim 21 is not allowed. Both the MPEP and the CFR provide that the Office Action must identify the specific teachings relied upon in support of a rejection of Applicant's claims.

In particular, Applicant respectfully requests identification *in a non-final action* of elements which allegedly correspond to limitations of the claims in accordance with 37 C.F.R §1.104(c)(2). 37 C.F.R §1.104(c)(2) provides that *the pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.* Further, 37 C.F.R. §1.104(c)(2) states that the Examiner must cite the best references at their command. When a reference is complex or shows or describes inventions other than that claimed by Applicant, the particular teachings relied upon must be designated as nearly as practicable. The pertinence of each reference if not apparent must be clearly explained for each rejected claim specified. Applicant respectfully requests clarification of the rejections with respect to specific references and specific references teachings therein pursuant to 37 C.F.R. §1.104(c)(2) in a *non-final Action* if any claims

are not found to be allowable.

Applicant again disagrees with the rejection of claim 21 over the '591 reference. The Office Action fails to comply with the MPEP and CFR. More specifically, the Office Action identifies the teachings of col. 6, lines 15-20 as allegedly teaching one series of FETs being isolated from adjacent devices by STI. The Office Action is in error. The identified teachings of col. 6 merely disclose that an insulation region defines a cell field for the non-illustrated memory cell configuration and is formed in a main area 2 of substrate 1 by LOCOS or STI. The disclosed "insulation region" of the '591 reference fails to disclose or suggest the claimed ***one series of FETs being isolated from adjacent devices by shallow trench isolation*** as claimed.

The erroneous nature of the rejection of claim 21 is further evident from the response to arguments section on page 5 of the Action wherein it is stated that the '591 reference does teach to form STI isolation structures and need to depict them in detail in the relevant figures in order to anticipate Applicant's claims. Initially, Applicant again refers the Examiner to the MPEP and CFR sections identified above and the mandate for specificity with respect to identification of reference teachings. Next, with respect to the argument than the '591 reference teaches STI isolation structures, Applicant has electronically searched the '591 reference and has failed to uncover any reference teachings with respect to "an isolation structure" let alone the specific "STI isolation structure" which the Office Action alleges is disclosed in the '591 reference. In col. 6, lines 52+ the '591 reference teaches insulation structures 7 however such structures are not disclosed as comprising STI isolation structures. The '591 reference does not disclose STI isolation structures as alleged in the Office Action.

The above deficiencies illustrate the tenuous nature of the Examiner's rejection of claim 21. Applicant again requests allowance of claim 21. In accordance with the CFR and MPEP, if claim 21 is not allowed Applicant specifically requests specific identification of the reference teachings which allegedly disclose *one series of* ***FETs*** *being isolated from* ***adjacent devices*** *by* ***shallow trench isolation*** as claimed. In particular, Applicant requests identification of the specific '591 reference teachings by reference number and specific portions of the specification for each of the following: the ***one series of FETs***; the ***adjacent devices***; and the ***shallow trench isolation providing the claimed isolation of the one series of FETs and adjacent devices***.

Further, with reference to the statements on page 5 of the Action with respect to "F", F is not variable for a range of widths as again erroneously alleged in the Action. F is understood as the smallest feature size that can be produced with a given technology process. Applicant refers the Examiner to the teachings in col. 1, lines 50-54 of the '591 reference wherein the definition of F is provided. Indeed, the '591 reference indicates F for the disclosed technology of the reference is 0.4 microns as set forth in line 27 of col. 6. F is only variable between entirely different processing technologies used for fabrication of devices. Once the technology is selected (e.g., F=0.4 microns in the '591 reference), F is fixed with respect to processing of all devices using the chosen process. The '591 reference specifically discloses usage of a 0.4 micron technology wherein F is equal to 0.4 microns. F does not change but is dictated by the technology being employed which defines the value of F.

The width of the trenches defined in the '591 reference and the spacing of the trenches are defined in the '591 reference to have a common distance equal to F. F is

not variable "for a range of widths" as alleged in the Office Action. The Office Action on page 3 identifies teachings in col. 4 as allegedly disclosing the claimed other series having active area widths greater than 1 micron. The teachings in col. 4 merely state that a memory cell having both planar and vertical MOS transistors are arranged on an area of $2F^2$ and the mean area requirement for each cell is F^2. Such defines the footprint or real estate and fails to provide any teachings of the active area having a width greater than 1 micron as claimed. The Examiner identifies the teachings in col. 6, lines 34-45 as allegedly disclosing the claimed one series of FETs being formed to have active area widths less than one micron to achieve lower threshold voltages than the other series. The teachings identified in col. 6, lines 34-45 merely disclose spacing and dimensions of trenches formed in the '591 reference. The Office Action fails to identify which structures allegedly correspond to the first and the second series of FETs. The series of FETs having the differently active area widths to provide different threshold voltages is not shown nor suggested by the prior art and claim 21 is allowable for at least this additional reason.

Once again, in accordance with the CFR and the MPEP, if claim 21 is not allowed, Applicant requests identification of reference numbers and specification teachings which allegedly disclose the one and the other series of FETs having active area widths greater and less 1 micron as claimed. At a minimum, the Examiner is requested to identify which of the FETs of the '591 reference are considered to correspond to the claimed one and other series of FETs as claimed so Applicant may appropriately respond.

Further with respect to claim 21, Applicant thanks the Examiner for identifying voltage threshold teachings of col. 3, lines 20-36. However, the mere reference to "voltage thresholds" of col. 3 fails to disclose or suggest the claimed *one series formed to have active area widths less than one micron to achieve lower threshold voltages than the other of the series*. In particular, the teachings of col. 3 refer to the different threshold voltages provided by gate dielectrics of different thicknesses with no reference to active areas or active area widths greater or less than 1 micron as claimed. The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)." Accordingly, the bald, cursory reference teachings regarding "threshold voltages" of the '591 reference fail to disclose or suggest the claimed limitations of claim 21. Claim 21 is allowable for at least this additional reason.

Numerous limitations of claim 21 are not shown nor suggested by the prior art and claim 21 is allowable for at least this reason.

The claims which depend from independent claim 21 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

Referring to claim 22, the Action on page 3 refers to the teachings of col. 6, lines 20-30 to allegedly anticipate limitations of claim 22. Applicant disagrees. Such teachings only refer to the formation of depletion regions 3 at the tops intermediate the trenches. However, the '591 reference fails to disclose or suggest *the depletion regions 3 corresponding to active areas of two series of transistors having active area widths*

greater and less than 1 micron, respectively. Further, the arguments on page 5 of the Action also fail to establish the implant of col. 6, lines 20-30 defining the different threshold voltages of the two series of transistors as claimed. Limitations of claim 22 are not shown nor suggested by the prior art and claim 22 is allowable for at least this addition reason.

If claim 22 is not allowed and in accordance with the mandate of the MPEP and CFR, Applicant respectfully requests identification of specific reference teachings including specification recitations and identification of reference numbers of the teachings of the '591 reference which are alleged to disclose the ***common channel implant defining the threshold voltages of the two series of FETs having active areas greater and less than 1 micron*** as claimed.

With reference to claim 23, the Examiner identifies the teachings of col. 7, lines 15-20 in support of the 102 rejection. The identified teachings only correspond to the vertical transistor configuration. The '591 reference is devoid of any teaching or suggestion that the common channel implant of the trench sidewalls defines different threshold voltages for plural series of FETs as claimed, or that such implant is the only implant which defines the threshold voltages as positively claimed. If claim 23 is not allowed and in accordance with the MPEP and CFR, Applicant requests specific identification by reference numbers in the Figures of the structures of the '591 reference which allegedly correspond to the claimed two series of FETs so Applicant may appropriately respond.

Referring to claim 24, *the '591 reference fails to disclose or suggest* ***any channel implants which are common to plural series of transistors having different***

threshold voltages as claimed. Claim 24 is allowable for at least this additional reason and Applicant requests clarification of any rejection of claim 24 in accordance with the CFR if claim 24 is not allowed.

With reference to independent claim 26, the '591 reference fails to disclose or suggest ***at least one series of FETs being isolated from adjacent devices by shallow trench isolation and the transistors having different threshold voltages*** as claimed. Claim 26 is allowable for at least this reason.

The '591 reference is also devoid of any teaching or suggestion of the claimed ***achieving different threshold voltages between FETs in different series by varying the active area widths of the FETs in the series***. Claim 26 is allowable over the '591 reference for at least this additional reason.

Applicant requests identification of specific teachings of the '591 reference if claim 26 is not allowed in the next Action in accordance with the MPEP and CFR so Applicant may appropriately respond.

The claims which depend from independent claim 26 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

Applicant submits herewith a copy of an IDS and form PTO-1449 which includes references which have not been initialed by the Examiner. Applicant requests initialization of the references on the 1449 and return of the form to Applicant.

Support for the new claims is provided at least by Figs. 3 and 4 and the associated specification teachings of the originally-filed application.

The Examiner is requested to phone the undersigned if the Examiner believes such would facilitate prosecution of the present application. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

2/23/04
Date

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